IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Tak M. Mak et al.	Examiner:	Saqib Javaid Siddiqui
Serial No.:	10/608,390	Group Art Unit:	2138
Filed:	June 26, 2003	Docket No.:	884.833US1
Title:	A PSEUDO BUS AGENT TO SUPPORT FUNCTIONAL TESTING		
Customer Number: 21186			

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

The applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a Notice of Appeal.

The review is requested for the reason(s) stated below:

§*103 Rejection of the Claims*

Claims 1-26 were rejected under 35 USC § 103(a) as being unpatentable over Kundu et al. (U.S. 6,510,398 B1) and further in view of Evans (U.S. 2003/0051197 A1). It is of course fundamental that in order to sustain an obviousness rejection that each and every step or element in the rejected claims must be taught or suggested in the proposed combination of references.

Kundu is directed to testing an integrated circuit and Evans is directed to testing a cache. Contrary to the assertion of the Examiner, Applicants respectfully assert that there is no teaching or suggestion of a teaching or suggestion of a teaching in Evans where there is a pseudo bus agent that emulates bus operations for cache paging operations.

The Examiner recognizes that Kundu does not address testing cache or cache page operations over a pseudo bus. Accordingly, the Examiner has relied on the teaching provided in Evans where cache operations are tested. However, Evans actually uses the bus of the machine to test cache misses and acquires data from registers during a cache miss. There is no concept of a pseudo bus agent that emulates bus operations. In fact, in Evans the bus is actually used, it is not emulated as the Examiner appears to assert.

More specifically, paragraph 37 indicates that the select line is a bus; FIG. 2 comports with this. The bus is an active part of the cache testing. FIG. 1 shows that the MISR includes lines that interact over a bus to a register to process cache misses. Paragraph 61 describes the MISR in more detail. There it can be seen that on a cache miss the MISR actually acquires data from a register via a bus or connection to the register. The MISR processes cache misses. The MISR does not emulate a bus transaction for a cache miss or cache page. In fact, there is no concept of a pseudo bus agent that is capable of emulating a bus transaction for a cache page operation. The approach used in Evans is to actually access a bus and a register to acquire data during a cache miss operation. This is not, as the Examiner asserts it to be, an emulated bus transaction. It is in fact a physical bus transaction to a register.

Accordingly, Applicants assert that Evans fails to teach an emulated bus transaction or a pseudo bus agent as the Examiner asserts. Applicants respectfully cannot find any remote teaching to this effect because Evans specifically teaches accessing a normal bus to acquire data from a register during a cache miss. This is not what Applicants have claimed. Therefore, the rejections should be withdrawn and the claims allowed. Applicants respectfully request an indication of the same.

Conclusion

Applicants respectfully submit that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicants' attorney at (513) 942-0224 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

TAK M. MAK ET AL.

By their Representatives,
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, Minnesota 55402
(513) 942-0224

By /__ Joseph P. Mehrle _____/
Joseph P. Mehrle
Reg. No. 45,535